WILEY-VCH

DOI: 10.1002/adfm.201400129
Article type: Full Paper

Printed Transistors on Paper: Towards Smart Consumer Product Packaging

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Keywords: paper substrate, locally printed smoothing layer, printed organic field effect transistors (OTFT), gravure printing, pBTTT

Abstract

The integration of fully printed transistors on low cost paper substrates compatible with roll-to-roll processes is demonstrated here. Printed electronics promises to enable a range of technologies on paper including printed sensors, RF tags and displays. However, progress has been slow due to the paper roughness and ink absorption. This is solved here by employing gravure printing to print local smoothing pads that also act as an absorption barrier. This innovative local smoothing process retains desirable paper properties such as foldability, breathability and biodegradability outside of electronically active areas. AFM measurements show significant improvements in roughness. The polymer ink and printing parameters are optimized to minimize ink absorption and printing artifacts when printing the smoothing layer. Organic thin film transistors (OTFT) are fabricated on top of this locally smoothed paper. OTFTs exhibit performance on par with previously reported printed transistors on plastic utilizing the same materials system (pBTTT semiconductor, poly-4-vinylphenol dielectric). OTFTs deliver saturation mobility approaching 0.1cm^2/V-s and on-off-ratio of 3.2E+4. This attests to the quality of the local smoothing, and points to a promising path for realizing electronics on paper.

1. Introduction

This work demonstrates printed transistors on paper that offer performance on par with plastic-based devices, while the attractive physical properties of paper are retained. This process can be integrated into traditional paper packaging process flows. Paper is one of the most ubiquitous materials in everyday life. It has been used for centuries to display printed information in addition to other applications. The reasons are manifold including the low cost of paper itself, the ability for high-throughput, low cost printing on paper, biodegradability, permeability, foldability and many more. There will be countless opportunities if these properties can be integrated with electronic functionalities. One of the most immediate applications is the integration of sensing, communication and display functionalities with paper consumer packaging. This cannot be achieved with traditional microfabrication, however, the advent of printed electronics offers the opportunity to close this gap.

Printed electronics is ideally suited for applications that require large-area, flexible substrates at minimal cost. Many different electronic devices and systems have been demonstrated including transistors[1–4], RFID tags[5,6], sensors[7,8], and displays[9]. However, most of these advances have been made on plastic substrates. Little progress has been made on paper. The largest roadblocks preventing this are the surface roughness and ink absorption due to the porosity of paper.[10] High resolution printing methods such as inkjet and gravure rely on relatively low viscosity inks, which are absorbed by standard paper. Higher viscosity inks cannot be printed by inkjet, but they can be printed by gravure. This makes gravure attractive for the printed multi-layer smoothing introduced here, however, fine lines printed with gravure directly onto paper would still suffer substantially from the large roughness of paper. So far this has prevented any fully printed devices or systems, compatible with paper packaging flows, from being demonstrated.

One previous approach has been to “hide” the paper under a blanket coating of a smooth material; coating methods such as spin coating[11–13] and parylene evaporation[14–16] have been

used to deposit thick smoothing layers. Unfortunately, such approaches are not viable for real packaging applications since all the attractive mechanical properties of paper, such as foldability, breathability etc., are lost when coated with blanket sealing layers. It is also undesirable from a cost perspective since large areas of paper are unnecessarily coated, wasting large quantities of material. Further, other previous work has made use of coated "inkjet paper" substrates[17], which are too expensive for use in consumer product packaging and don't have sufficient thermal stability for some higher temperature fabrication processes. There have also been reports of devices fabricated directly on paper. This is mostly done by conventional micro fabrication techniques such as sputtering or vacuum deposition thereby avoiding the problem of ink absorption into paper during printing.[18,19] Whilst this might be viable for some niche applications such as security features on banknotes, it won't meet the cost requirements of most applications of paper electronics. Direct printing on paper using screen printing has also been attempted, however, with relatively large channel lengths (200μm),[20] which highlights the challenges involved in the scaling of printed transistors on rough paper. This can be acceptable for certain applications such as low resolution electrothermochromic displays.[21] However, most electronic applications will require high resolution printing of scaled transistors. Overall, therefore, existing processes and techniques are generally not viable, since they are incompatible with conventional packaging flows, which make use of printing techniques and run in high-speed roll-to-roll processes on low-cost paper stock.

These challenges are overcome by the integrated process flow demonstrated here. A smoothing underlayer as well as overlying transistors are printed on low-cost paper using gravure printing. Gravure printing is widely used in graphic arts, and therefore, this work is a natural evolution of consumer product packaging to integrate printed transistors. The smoothing layer is printed locally as defined by the pattern on the gravure roll. This preserves the desirable properties of paper outside of the electronically active areas, which can be a

small fraction of the overall size of the paper. Interconnects between multiple smoothed regions with high performance devices could then be fabricated by methods such as screen printing, or indeed, using lower-resolution gravure printing of more viscous (and thus less absorbed) conductor inks, since high resolution printing would be less of a concern.
Printed smoothed pads are shown to exhibit significantly improved properties as a substrate for printed electronics compared with bare paper while allowing the paper substrate in general to retain its desirable mechanical characteristics. Printed capacitors and transistors were fabricated in smoothed regions. These devices exhibit performances on par with devices previously reported on plastic substrates, attesting to the robustness of the paper integration. **Figure 1** shows printed transistors on locally smoothed pads demonstrating both high quality printed features as well as the truly local nature of smoothed pads.

2. Fabrication processes

The paper used here is a low-cost smoothed paper from Stora Enso, a large producer of packaging materials. The paper is formed from wood fibers and is coated by Stora Enso with kaolin (clay) as an initial smoothing layer. The final smoothing layer was gravure printed using poly-4-vinylphenol (PVP) dissolved in propylene glycol monomethyl ether acetate (PGMEA) and later cross-linked with poly melamine-co-formaldehyde methylated at 210°C. To evaluate dielectric and conductor performance, capacitors were fabricated by inkjet printing the bottom and top electrodes and gravure printing the PVP gate dielectric. Electrodes were printed with a commercial silver nanoparticle ink (CCI-300), which was sintered at 150°C. The gate dielectric was printed with a similar PVP ink as the smoothing layer but with lower viscosities to control the printed thickness of thin gate dielectric layers. Bottom-gate, bottom-contact organic thin-film transistors (OTFTs) were fabricated in the same manner using a spun poly(2,5-bis (3-tetradecyl-thiophen-2-yl)thieno[3,2-b]thiophene) (pBTTT) semiconductor layer on top, cured at 160°C and cooled slowly to aid crystallization of large grains. Spin coating was chosen

because it could be performed under an inert nitrogen atmosphere. However, OTFTs with printed pBTTT have been demonstrated in the past[3] making this a fully printable process flow. Before semiconductor deposition, the source/ drain and gate dielectric were exposed to 10 minutes of UV ozone treatment, which has been found to improve transistor performance. All transistor measurements were conducted under a nitrogen atmosphere. The TFT fabrication process flow is illustrated in Figure 1.

3. Paper characterization with and without smoothing

The paper substrate used in this study was analyzed to identify its strengths and weaknesses as a substrate for printed electronics. The thermal budget that a substrate can withstand is a crucial parameter for any microelectronic fabrication process. It was found that this paper outperforms many low cost plastic substrates in terms of thermal stability.

Substrate roughness is a key consideration for device performance, affecting parameters such as line edge roughness and dielectric breakdown strength. This had to be improved significantly from the original paper and was achieved by gravure printing of a polymer smoothing layer.

Ink absorption by the substrate is another crucial parameter for successful printing. This was also improved significantly by the smoothing layer.

With these key improvements the paper became a viable substrate to be used for fully printed high performance electronics.

3.1. Temperature stability

The thermal budget of the paper substrate was characterized qualitatively in terms of darkening and mechanical degradation and quantitatively by thermogravimetric analysis (TGA) (**Figure 2**). Qualitatively, first signs of degradation are observed at about 250°C and TGA confirms that no significant degradation occurs below 300°C. This is higher than all low-cost plastics and photo papers, and attests to the viability of kaolin coating to produce highly stable

paper substrates for printed electronics. It is certainly compatible with organic electronics and, in the future, might also allow the use of solution processed inorganic materials with higher temperature requirements.[22]

Similarly, the PVP smoothing material was analyzed to find its maximum processing temperature. Degradation of cross-linked PVP begins at approximately 210°C (Figure S1). This is sufficient for organic electronics, but could be improved in the future to fully utilize the thermal capabilities of the paper.

3.2. Roughness and smoothing layer printing optimization

One of the major roadblocks preventing the usage of paper as a substrate for printed electronics is the large roughness and absorption of fibrous paper. **Figure 3** shows an atomic force microscopy (AFM) image of paper as received. It is clear that this micrometer-scale peak-to-peak roughness would be unacceptable for active layer thicknesses on the order of 10s to 100s of nanometers. This problem was resolved with a gravure printed PVP smoothing layer; the use of a printed local smoothing layer allows for creation of smooth regions in the electronically relevant areas, while ensuring that the paper largely retains its intrinsic properties. Figure 3 shows the significant improvements that were achieved. The improvement in roughness was quantified by the peak-peak roughness extracted from AFM scans (30µm x 7.5µm).

The first smoothing layer printing parameter to be studied was ink viscosity, which was varied by changing the polymer concentration dissolved in the solvent. The printing speed was varied at the same time as the ink viscosity to maintain a constant capillary number $\left(Ca = \frac{Viscosity * Speed}{Surface\ tension}\right)$ to keep printing conditions constant.[23] Two different regimes can be observed (**Figure 4**). For low viscosities the ink is simply absorbed by the paper without achieving significant smoothing of the paper. For high viscosities roughness is increased by printing artifacts. Figure 4 (b) shows how these artifacts manifest themselves as holes in the

PVP film. Optical measurements with a larger field of view than AFM confirm that the lateral and vertical size of these voids increases with increasing ink viscosity as suspected from AFM. This type of printing artifact is not unique to printing on paper and also occurs on plastic substrates (polyethylene terephthalate (PET), see Figure S2). High viscosity ink was printed on PET with different gravure cell spacing to investigate the cause of these voids. The size of voids increases with increasing cell spacing ultimately leading to isolated drops of size comparable with the cell size (see Figure 4 (c)). This suggests that voids are not caused by printing instabilities but rather due to insufficient spreading of high viscosity inks during drying. The optimum ink viscosity was found to be approximately 150cP.

The effect of gravure cell size and the number of PVP layers was investigated using ink with optimized viscosity. Not surprisingly, roughness decreases with increasing cell size and number of layers due to the larger volume of ink deposited per unit area (see **Figure 5**). The decrease with number of layers follows a non-linear trend leading to diminishing returns for large numbers of layers. This can be understood from cross-sectional images (see Figure 5 (a)). For one and two layers of smoothing one cannot make out a continuous PVP layer because not all pores in the paper are filled. For three, four and five layers one can extract a thickness of the PVP layer (see Figure 5 (b)). This follows a linear trend. For each additional layer the already printed PVP, which is not cross-linked yet, is re-dissolved and thus allowed to penetrate the paper further. This explains why the improvements in smoothing diminish once three layers have been printed. The linear trendline can be extrapolated to cross the x-axis in between 2 and 3 layers. This suggests that there will be no continuous PVP layer for fewer than three layers, which is also observed in the cross-sectional images.

Therefore the optimum number of smoothing layers was found to be three and this was used for all further substrate characterization and device printing. Three layers of PVP were printed

with the largest cells available here (45μm cell depth), with an ink viscosity of 150cP and with a printing speed of 0.1m/s giving a capillary number of 0.5.

3.3. Printing on smoothed paper

Absorption of low viscosity inkjet inks is a major problem for printed electronics on paper. **Figure 6 (a)** shows water being absorbed and permeating through untreated paper within less than 30 seconds. Paper treated with PVP shows no significant absorption. The only reduction in drop volume is due to evaporation comparable to a drop on PVP coated plastic.

The contact angle of inks with the substrate is another important parameter in determining printing performance. Untreated paper exhibits a very low contact angle in part due to lateral absorption and spreading. Paper treated with PVP exhibits a water contact angle similar to PVP spun onto PEN (see Figure 6 (b)), which suggest that printing performance on these substrates will be comparable.

Printing high definition features on PVP is routinely done in OTFT fabrication on plastic substrates where PVP is used as a gate dielectric or as a substrate planarization layer.[24] Figure 6 (c) compares inkjet printed silver lines on bare paper and on smoothed paper. Problems with absorption and irregular features are evident on the bare paper. Conversely the smoothed paper exhibits perfect features only limited by the accuracy of the printer.

4. Device performance

4.1. Dielectric scaling

Metal-insulator-metal capacitors (MIM) were fabricated on the smoothed paper to verify satisfactory performance of the gate dielectric on this initially rough substrate (see **Figure 7 (a)**). The dielectric thickness was scaled by varying the ink viscosity for gravure printing of the PVP dielectric (Figure S3). Ink viscosity was controlled by the amount of PVP dissolved in PGMEA. Dielectric breakdown was defined as the voltage producing a leakage current density of 10^{-5}A/cm^2 because hard breakdown only occurs at large fields (Figure S4). This current

density corresponds to a projected TFT on-off ratio of 10^4.[25] It was found that the breakdown field as defined by leakage does not suffer when the dielectric is scaled, however, device yield does decrease somewhat (see Figure 7 (a)). MIM capacitors were also fabricated on paper smoothed with more layers of PVP (4 and 5). It was found that this does not alter leakage behavior significantly demonstrating that 3 layers of smoothing are sufficient (Figure S5).

4.2. TFT performance

Organic TFTs were fabricated with the same process as for the thinnest gate dielectric. Figure 7 shows typical I_D-V_{GS} and I_D-V_{DS} curves. Transistor parameters were extracted from 15 devices and the mean was compared to values from previous works with the same dielectric and semiconductor materials on plastic substrates.[3,4] It was found that transistors on paper exhibited comparable behavior to transistors on plastic, except for showing degraded swing (see Table 1). This attests to the quality of the paper smoothing process proposed here.

4.3. Bending tests

Most applications for printed systems on paper will require flexible and bendable electronics. The mechanical robustness of the devices fabricated here was thus investigated under bending. A series of cylindrical dowels was used to define controlled bending radii. A PEN carrier was used to facilitate handling. This leads to a larger strain in the devices compared to just bending the paper to the same radius. The Young's moduli of both paper and PEN were measured. Treating the sandwich as a composite beam with no uniaxial tension or compression, the strain in the devices and an equivalent bending radius for just bending the paper without a carrier were calculated (see supplementary information for further details).

TFTs on paper were strained in the direction parallel to current flow. No significant device degradation within the measurement error and device-to-device variation could be observed up to a strain of 2.2% (equivalent bending radius 1.59mm). The paper itself tore when bent to the next smaller radius. **Figure 8 (a)** shows the evolution of saturation mobility under bending, which reveals no significant degradation upon bending. Other parameters showed similar

behavior. This confirms that this device structure is robust against bending up to the failure point of the paper.

Under stress in the direction perpendicular to current flow, the most likely failure mechanism would be cracking of the electrodes. The sheet resistance of the printed silver lines was measured as a function of bending and again no significant degradation could be observed (see Figure 8 (b)). These results attest to the robustness of printed electronics on paper under bent conditions.

5. Conclusions

We demonstrate that roll-to-roll printing can overcome major roadblocks towards printed electronics on paper. A locally printed smoothing underlayer was shown to tremendously improve surface roughness, ink absorption and printability whilst preserving desirable paper properties in unsmoothed regions.

Printed transistors were fabricated on low-cost paper using this technique, and were shown to exhibit performance comparable to similar transistors on a plastic substrate that had been reported previously. Robustness of devices to bending was also demonstrated. This thus represents an important step towards the realization of smart consumer packaging integrating printed circuits directly onto packaging stock.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors acknowledge Stora Enso for providing the initial paper substrates. Funding was provided by the Sharp Laboratories of America and the UC Discovery Program.

Received: ((will be filled in by the editorial staff))
Revised: ((will be filled in by the editorial staff))
Published online: ((will be filled in by the editorial staff))

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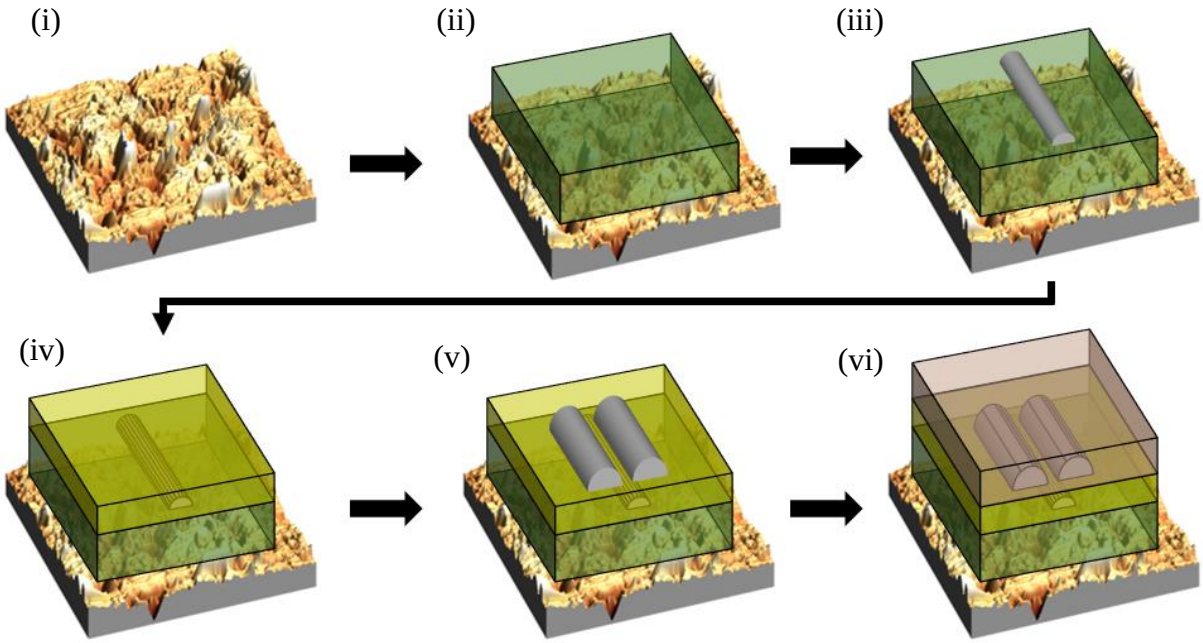
(a)



(b)

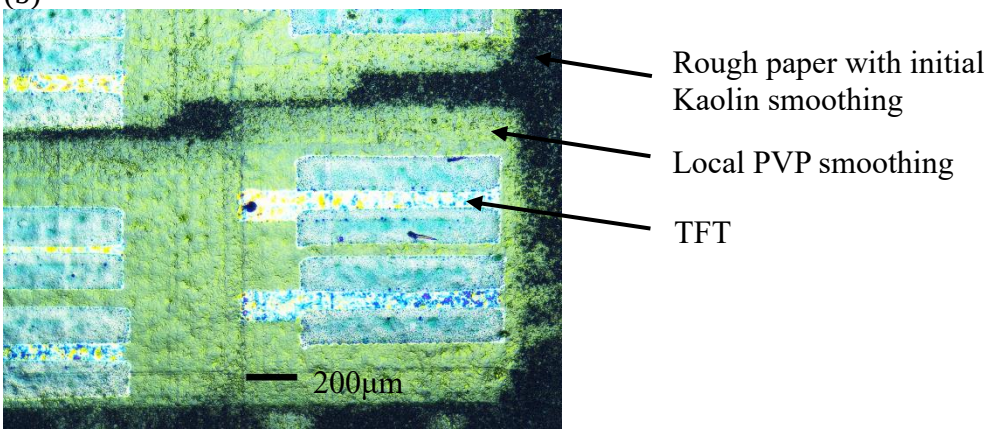
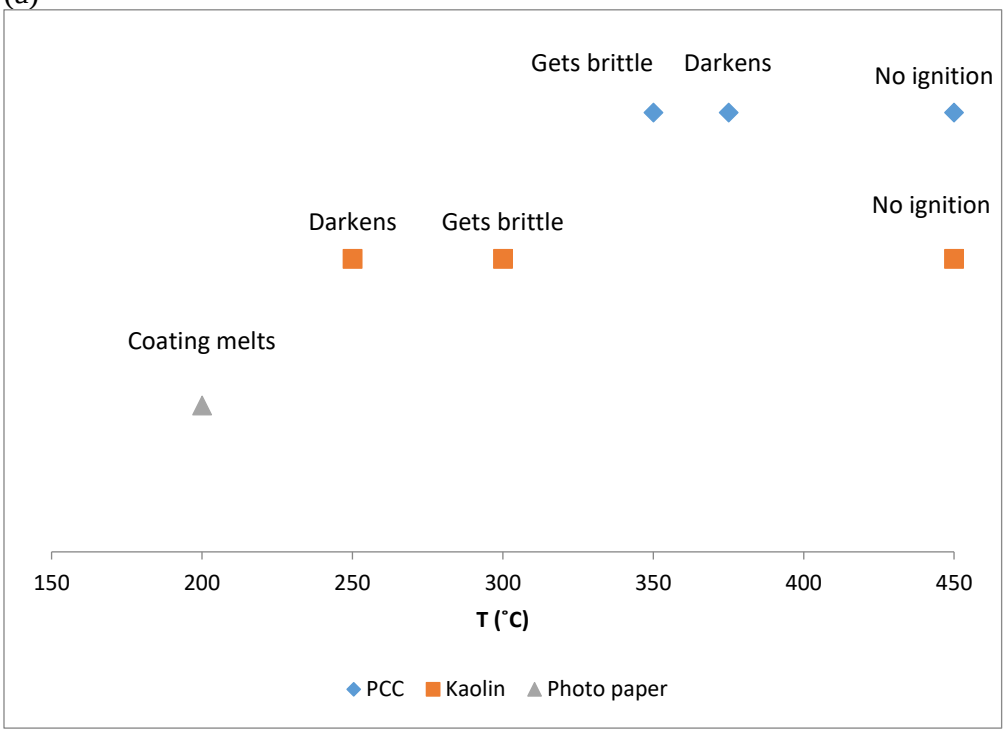


Figure 1. (a) Schematic illustration of TFT process flow. The process flow is identical for MIM capacitors except that the last semiconductor deposition step is omitted and the electrodes are fully overlapped. (i) Rough paper with initial Kaolin smoothing. (ii) Gravure print local smoothing poly-4-vinylphenol (PVP), cross-link 210˚C 30 minutes. (iii) Inkjet print bottom gate silver (CCI-300), sinter 150˚C 30 minutes. (iv) Gravure print PVP gate dielectric, cross-link 210˚C 30 minutes. (v) Inkjet print source and drain silver (CCI-300), sinter 150˚C 30 minutes. (vi) UVO 10 minutes, Spin coat pBTTT C16, Anneal 160˚C 10 minutes, Cool slowly. (b) Optical micrograph of fully printed transistors on locally printed PVP smoothing (bright pads). The unmodified paper is visible as the dark areas surrounding smoothed pads.

(a)



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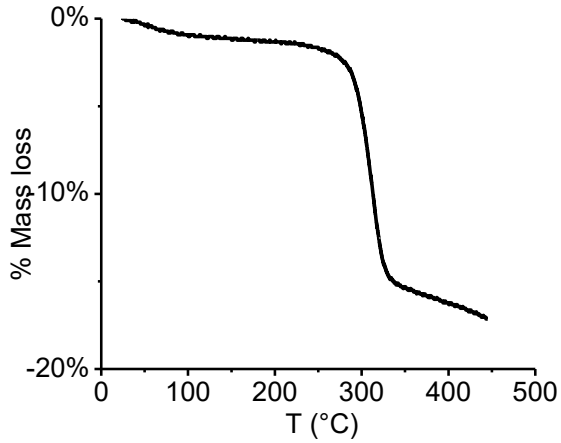
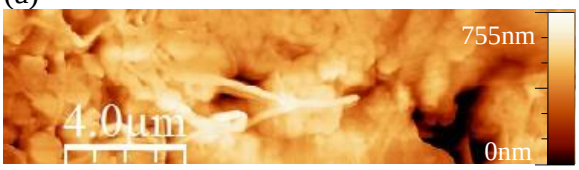


Figure 2. (a) Qualitative paper degradation with temperature for three different papers: Precipitated calcium carbonate (PCC) smoothing, Kaolin smoothing and conventional photo paper. Kaolin-smoothed paper being used throughout this work. (b) TGA of kaolin coated paper confirming qualitative result. No significant degradation can be observed below about 300˚C.

(a)

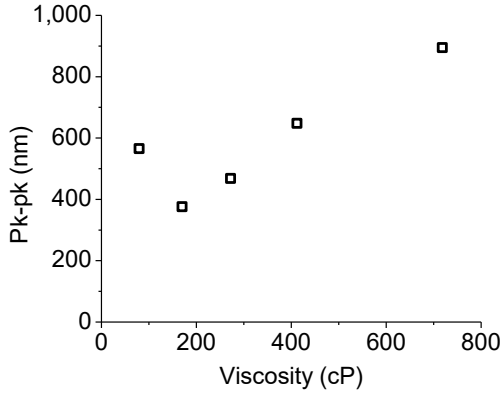


(b)

(c)

Figure 3. AFM topography scans of the paper (a) before and (b) after the PVP smoothing layer is applied both shown on a similar data scale. Image (b) is shown again on a finer data scale in (c) revealing some remaining long wavelength roughness.

(a)



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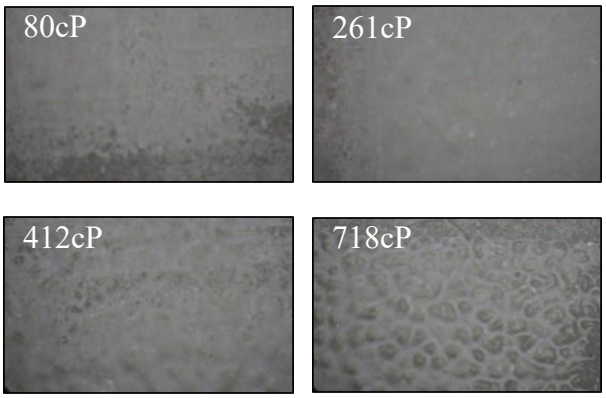

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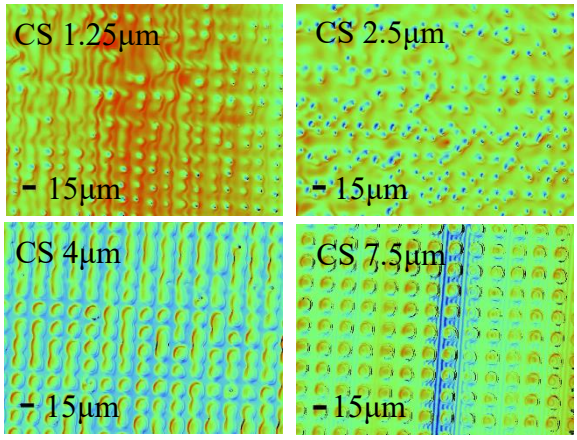


Figure 4. (a) Roughness optimization with PVP viscosity showing optimal smoothing at intermediate viscosities (5 layers of PVP). (b) Optical micrographs showing absorption of ink for low viscosity ink and increasingly large printing artifacts with increasing ink viscosity (5 layers of PVP). (c) Optical profilometry images for different cell spacing (CS) with constant cell size 15µm printed on PET (1 layer of PVP). The increased size of holes in the film with increasing cell spacing, ultimately leading to isolated drops of the same size as the cells, confirms that printing artifacts are due to high viscosity inks (here 2500cP) not being able to flow between cells before drying.

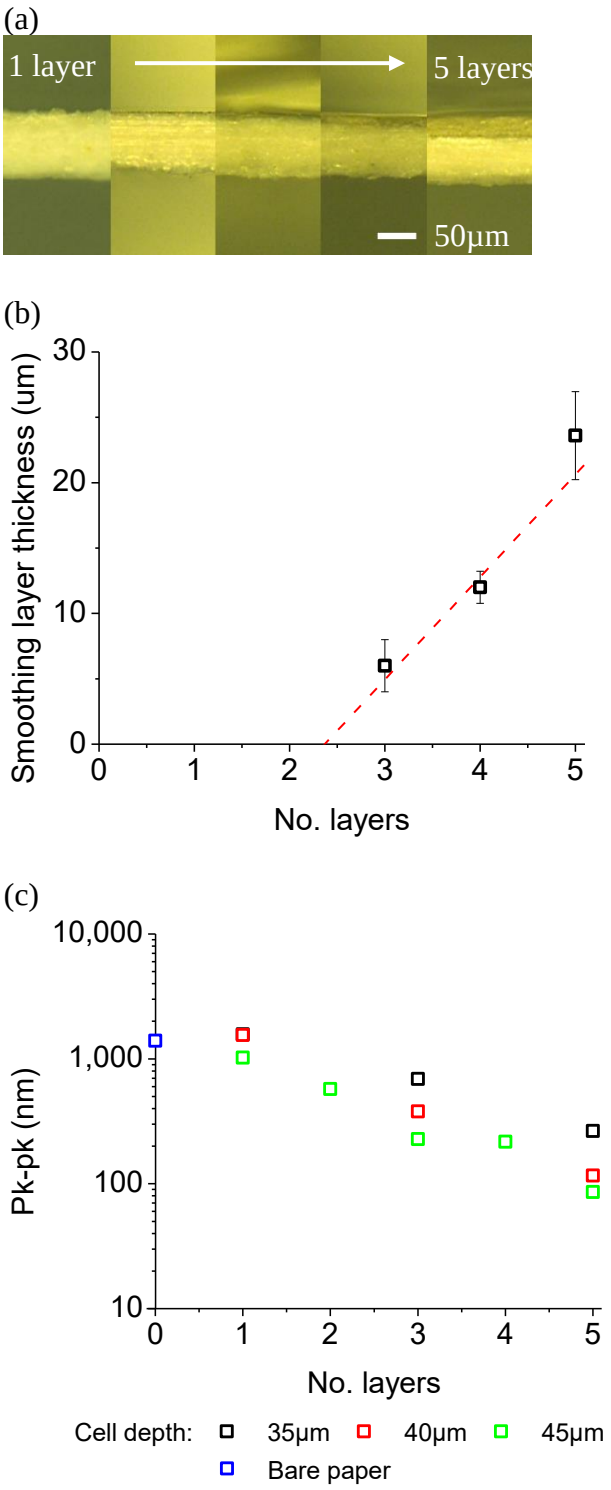
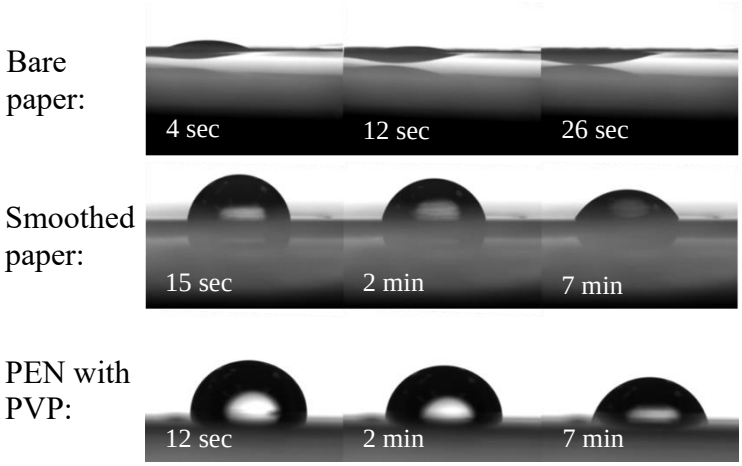


Figure 5. (a) Cross-sectional optical micrographs of paper smoothed with an increasing number of PVP layers. A continuous smoothing layer becomes visible for 3 or more layers. (b) The thickness of the smoothing layer increases linearly with number of smoothing layers. Extrapolation of the trendline confirms that no continuous layer is to be expected for fewer than 3 layers. (c) Pk-pk roughness with optimized ink viscosity (140cP) showing improved roughness with increasing cell depth and number of layers. The cells here were larger than the cells used to obtain the results in Figure 4 (a) further confirming the importance of large cells.

(a)



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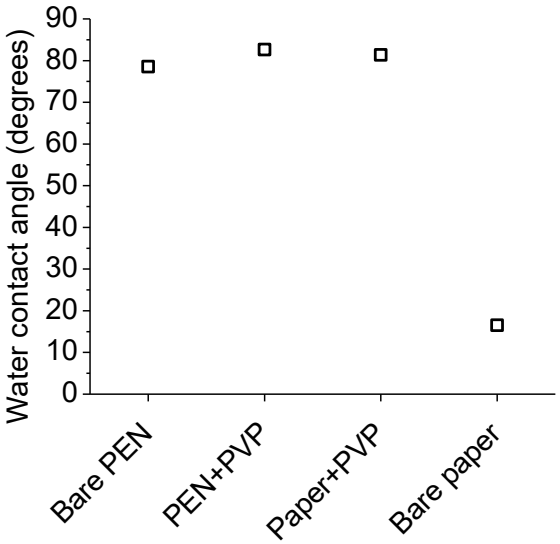

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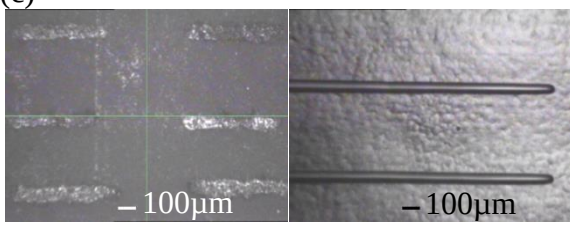
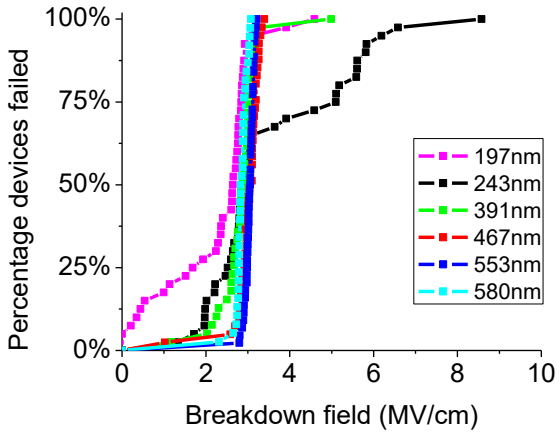


Figure 6. (a) Water absorption into bare paper and paper smoothed with PVP. Smoothed paper shows no significant absorption and only exhibits evaporative loss comparable to PEN coated with PVP. (b) Water contact angle is comparable on paper smoothed with PVP, PEN with spun PVP and bare PEN. This suggests good print quality on top of the smoothed paper since fine features are routinely printed on top of PVP. Bare paper exhibits a very low contact angle due to lateral absorption. (c) Optical micrograph of silver lines printed by inkjet on bare paper (left) and on smoothed paper (right). Ink is absorbed uncontrolledly by bare paper whereas smoothed paper allows good control over printed features.

(a)



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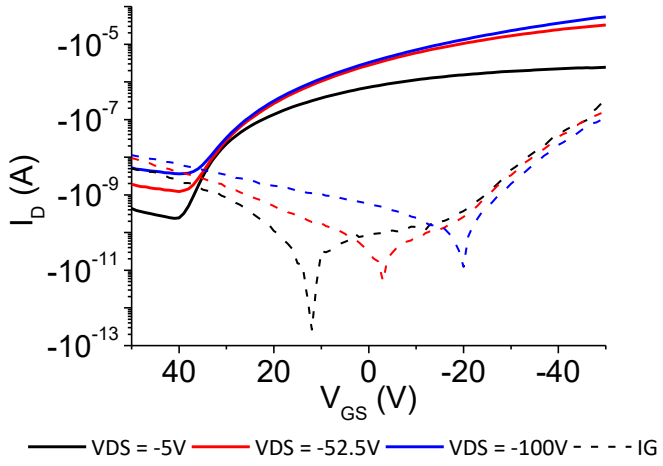


(c)

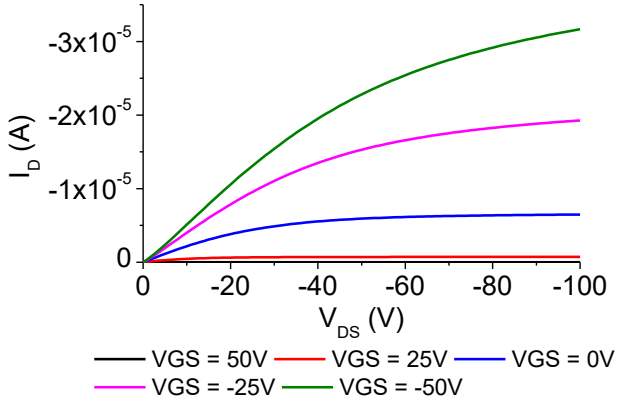
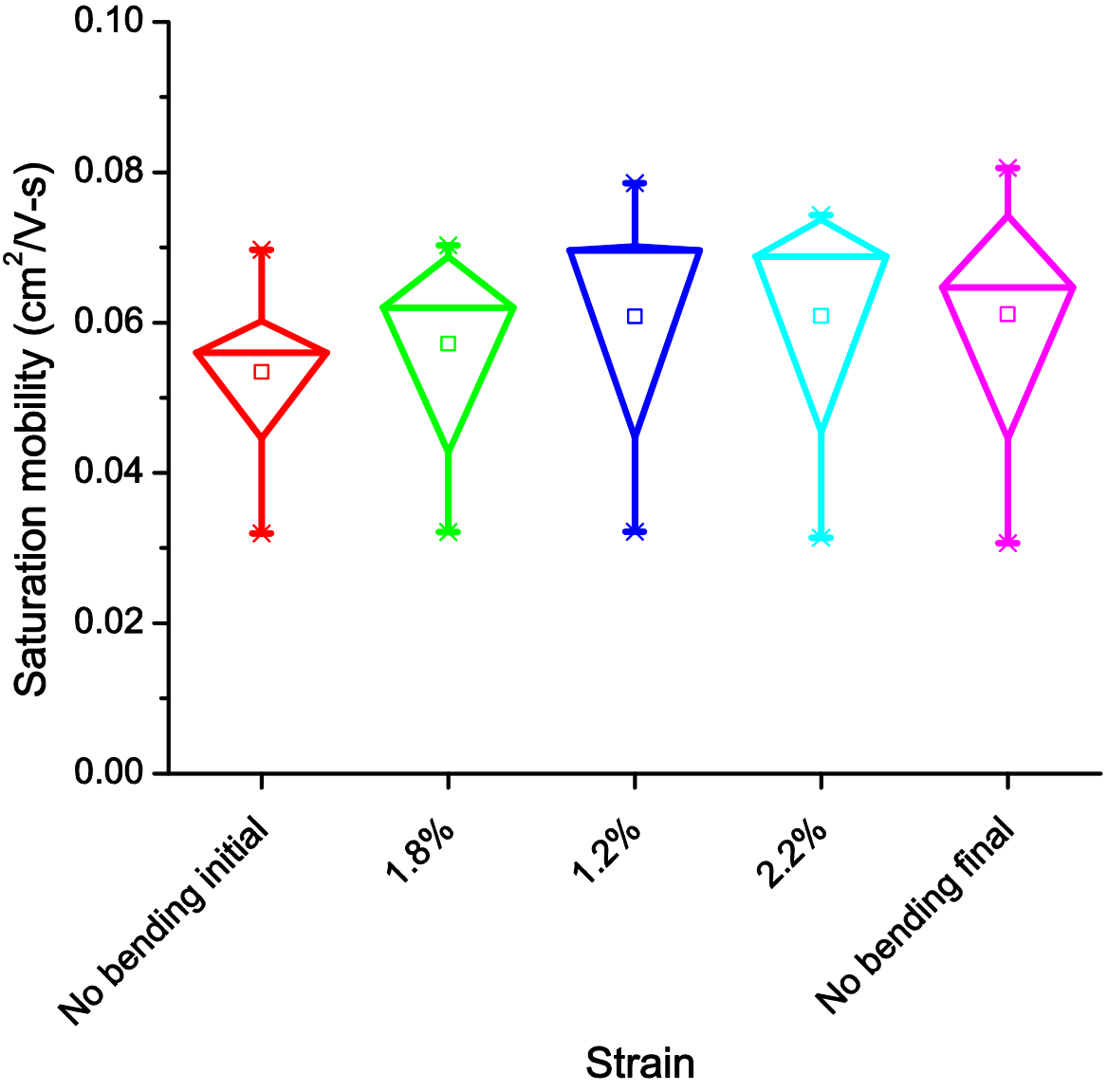


Figure 7. Printed device performance on smoothed paper. (a) Cumulative breakdown plot for MIM capacitors of different dielectric thicknesses exhibiting a consistent breakdown field for different dielectric thicknesses. (b) Typical I_D-V_{GS} characteristic. W/L=800µm/25µm. (c) Typical I_D-V_{DS} characteristic. Same device as in (b).

(a)


0.10
0.08
0.06
0.04
0.02
0.00
Saturation mobility (cm²/V-s)
No bending initial
1.8%
1.2%
2.2%
No bending final
Strain

(b)

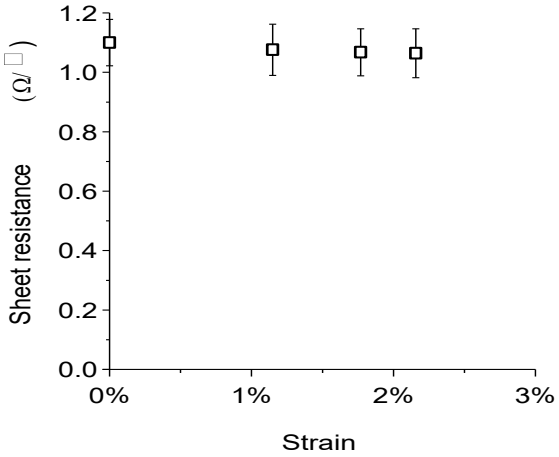


Figure 8. (a) Saturation mobility box plots under bending and unbent before and after bending showing no significant degradation under bending. Conditions are plotted in the same order that the experiment was conducted in. Here samples were treated with only 5 minutes of UVO instead of 10 minutes leading to slightly lowered mobility. (b) Sheet resistance of silver lines under bending confirming robustness to bending.

Table 1. Comparison of TFT characteristics with values from previously reported transistors on plastic with the same semiconductor and dielectric materials. Performance on par with devices on plastic confirms viability of the paper smoothing process proposed here.

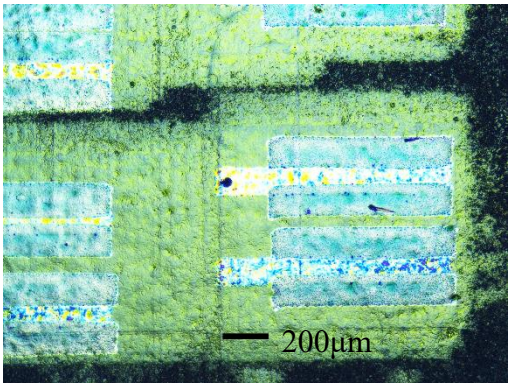
	This work	[3]	[4]
Saturation mobility (cm^2/V-s)	8.6E-2	1.5E-2	7.35E-2
Linear mobility (cm^2/V-s)	1.7E-2	2.6E-2	3.19E-2
On-off ratio	3.2E+4	3.7E+5	6.96E+2
V_{th} (V)	+0.88	-4	+5
Swing (V/dec)	18.1	9.5	5.48

Fully printed transistors are demonstrated on paper substrates with performance on par with plastic based devices. Desirable paper properties such as foldability, breathability and biodegradability are preserved outside of electronically active areas by an innovative locally printed smoothing process (see white smoothing area in figure). This process is fully compatible with existing paper packaging process flows.

Keywords: paper substrate, locally printed smoothing layer, printed organic field effect transistors (OTFT), gravure printing, pBTTT

G. Grau, R. Kitsomboonloha, S. L. Swisher, H. Kang and V. Subramanian*

Title: Printed Transistors on Paper: Towards Smart Consumer Product Packaging



Supporting Information

Printed Transistors on Paper: Towards Smart Consumer Product Packaging

*Gerd Grau, Rungrot Kitsomboonloha, Sarah L. Swisher, Hongki Kang and Vivek Subramanian**

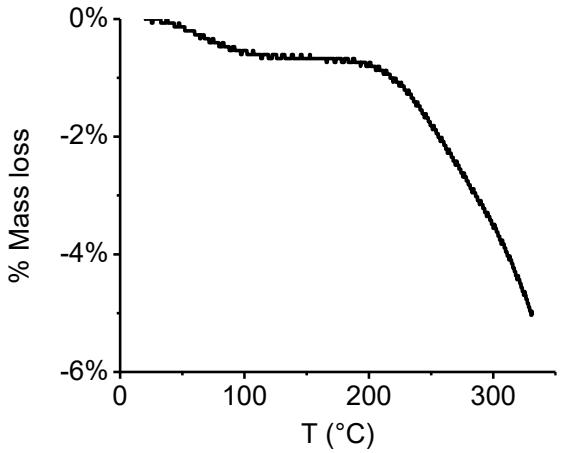


Figure S1. TGA of cross-linked PVP confirming sufficient thermal stability to allow organic electronics to be fabricated on top.

Figure S2. Optical micrograph of printing artifacts on plastic (PET) confirming that printing artifacts are independent of substrate (7 layers of PVP, 718cP).

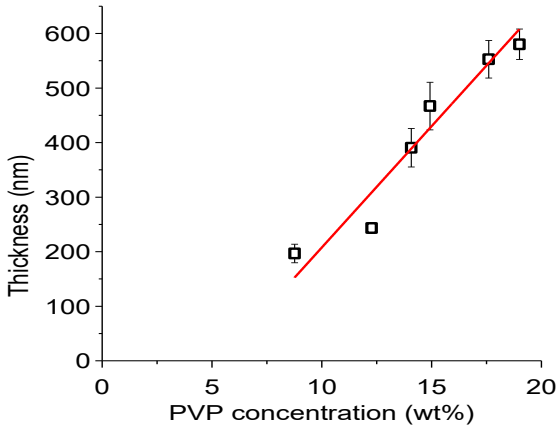


Figure S3. Dielectric thickness as measured from MIM capacitance is controlled by the concentration of PVP dissolved in the solvent for gravure printing.

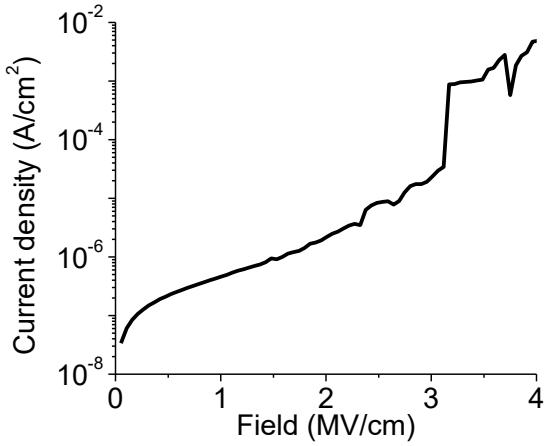
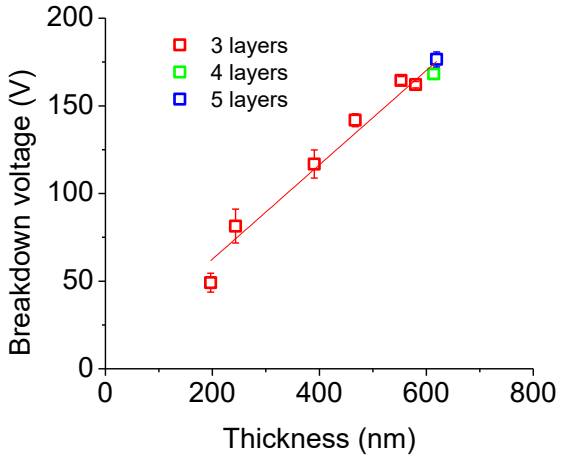


Figure S4. Typical leakage J-E-curve for 190nm dielectric.

(a)



(b)

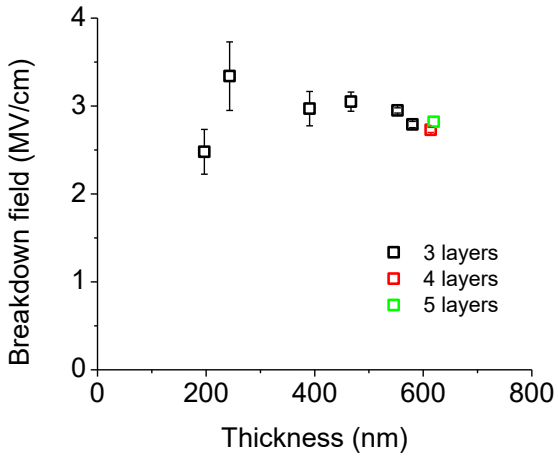


Figure S5. Average breakdown (a) voltage and (b) field vs dielectric thickness showing no dependence of breakdown field on dielectric scaling. Data points for 4 and 5 layer smoothing demonstrate that reduced roughness for these samples does not change breakdown field significantly.

The strain in the device layer and equivalent bending radius for bent paper without a PEN plastic carrier are calculated by treating the PEN-paper stack as a composite beam without any uniaxial tension or compression. The thicknesses of both the paper and the PEN were measured (t_{PAP}=70µm, t_{PEN}=130µm). The respective Young's moduli were measured through tensile tests (E_{PAP}=1.8GPa, E_{PEN}=4.75GPa). Composite beam theory then gives the following formulae for the distance of the neutral axis from the device layer on top of the composite beam y, the strain in the device layer ε_{device} and the equivalent bending radius for bending of paper without a plastic carrier R_{equiv}:

$$y = t_{PEN} + t_{PAP} - \frac{\frac{t_{PEN}^2}{2}\frac{E_{PEN}}{E_{PAP}} + \left(\frac{t_{PAP}}{2} + t_{PEN}\right)t_{PAP}}{\frac{E_{PEN}}{E_{PAP}}t_{PEN} + t_{PAP}} \quad \text{(S1)}$$

$$\varepsilon_{device} = \frac{y}{R_{dowel} + t_{adhesive} + t_{PEN} + t_{PAP} - y} \quad \text{(S2)}$$

$$R_{equiv} = \frac{t_{PAP}}{2}\left(\frac{1}{\varepsilon_{device}} - 1\right) \quad \text{(S3)}$$

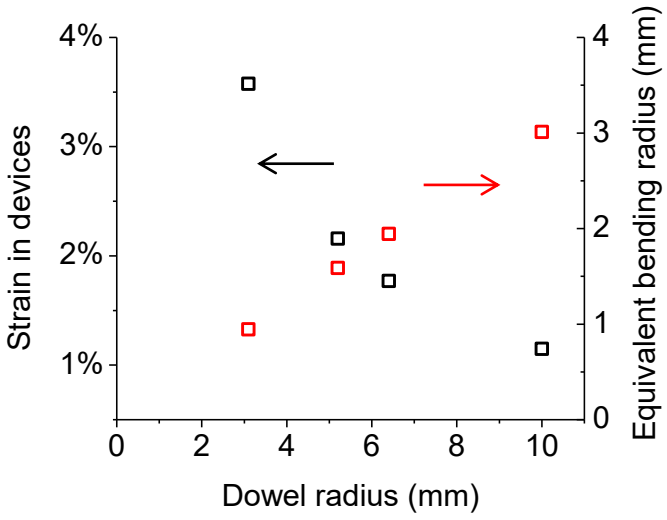


Figure S6. Strain in device layer and equivalent bending radius for paper-only bending compared to paper-plastic sandwich.